Errata

netX 51/52

STEP A and B

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1 Introduction

1.1 About this document

This document lists known errors and solutions/workarounds for netX 51/52.

1.2 List of revisions

Rev	Date	Name	Chapter	Revision
1	2013-05-22	AO/HH	all	Created
2	2014-06-10	IO/HH	2.3	Added
3	2015-01-15	BS/HH	2.4	Added
4	2015-07-22	HN	2.5	Added

Table 1: List of revisions

1.3 Affected silicon revision

netX	Revision/STEP	ROM Code Revision	Boot Loader Major Version
netX 51	A	3	0x43
	B	3	0x43
netX 52	A	3	0x43
	B	3	0x43

1.4 Errata overview

No.	Description
1	QSPI/SQI interface: Receiving data in mode 1 and 3
2	DPM interface: Ready generation during read access
3	EXT_... and HIF_ASYNCMEM_CTRL.Adr_ext_rdy_status.rdy_to_err
4	QSPI: Mode 0 and 2 of half-duplex receive mode in standard Motorola SPI (1-bit) mode are not working properly
5	HIF: Max. MISO hold time is 25 ns at SPI/SQI clock frequencies below 20 MHz (serial DPM)

2 Errata details

2.1 QSPI/SQI interface: Receiving data in mode 1 and 3

Issue

Mode 1 and 3 are not working properly in Dual and Quad SPI mode receive operation.

In Dual and Quad SPI modes 1 and 3 (i. e. ‘sqi_cr0’ register bit ‘sck_phase’ = 1) receive data could be lost when the receive FIFO runs full and the SQI module is in peripheral mode (i. e. register ‘sqi_sqirom_cfg’ bit ‘enable’ = 0).

Solution/Workaround

One of the following methods can be used to avoid this problem:

1. Use mode 0, if the connected device supports it.
2. For reading, use SQIROM mode 3 instead of SQI mode 3, if the connected device allows it, e. g. flash devices.
3. Only program transfers with a maximum of 64 bytes (i. e. the maximum FIFO size) and read out all data from the FIFO before programming a new transfer.

Operations and modes that are not affected by this problem

- Receive operation in Dual and Quad SPI, modes 0 and 2
- Receive operation in Dual and Quad SPI, modes 1 and 3 if receive FIFO getting full is avoided
- SQIROM/XiP, mode 0 and 3
- Transmit operation in Dual and Quad SPI, all modes
- Standard SPI, all modes

2.2 DPM interface: Ready generation during read access

Issue

Ready generation during a read access following a write access is not correct in case that the write access goes into an undefined (unmapped) area. I. e. the write address is upside the last configured dual-port memory data window on the netX side, which is called “bad” write access here.

The ready signal of the read access goes active before valid read data is put on the data signals.

- All following read accesses are processed correctly with correct ready behaviour. Only the first read access after the “bad” write access fails.
- The „bad“ write access itself is ignored internally.
- A write access after the „bad“ write access is processed correctly.
- For the erroneous read access a read error is flagged via bit 1 in DPM_STATUS register.

Operation and mode that is affected by this problem

- Parallel DPM modes that use ready signal
  (register DPM_RDY_CFG.RDY_DRV_MODE<>0).

Operations and modes that are not affected by this problem

- Parallel DPM modes that do not use the ready signal
  (register DPM_RDY_CFG.RDY_DRV_MODE=0),
- Serial DPM.

Solution/Workaround

One of the following methods can be used to workaround this problem:

1. Avoid writing into undefined (unmapped) areas.
2. Configure the minimal read access time on host side in a way that the read access after the “bad” write access also works without ready signal.

2.3 EXT_... and HIF_ASYNCMEM_CTRL.Adr_ext_rdy_status.-rdy_to_err

Issue (Bug)

The EXT_ASYNCMEM_CTRL.Adr_ext_rdy_status.rdy_to_err and the HIF_ASYNCMEM_CTRL. Adr_ext_rdy_status.rdy_to_err bit is cleared sometimes by reading the register. This doesn't happen always, because it depends on the applied, unpredictable data on the write data bus during a read access. Hence the bit is only valid for the first read after a timeout was detected. To clear the bit definitively a '1' must be written. The bit will never be lost without an access to this register.

Solution/Workaround

Read only one time after a timeout was detected.

2.4 QSPI: Mode 0 and 2 of half-duplex receive mode in standard Motorola SPI (1-bit) mode are not working properly

Issue (Bug)

Later transfers could fail, if SPI mode 0 or 2 is selected (i.e. ‘sqi_cr0’ register bit ‘sck_phase’ = 0) in standard Motorola SPI (1-bit) mode (i.e. the sqi_tcr register bits ‘mode’ = ‘00’) and a transfer is started in half-duplex receive mode (i.e. sqi_tcr register bit ‘start_transfer’ bit is set to ‘1’ with ‘duplex’ sqi_tcr register bits = ‘01’).

In that case the following error may occur: A later standard Motorola SPI (1-bit) send transfer (i.e. sqi_tcr register bit ‘start_transfer’ bit is set to ‘1’ with the sqi_tcr register bits ‘mode’ = ‘00’ and ‘duplex’ sqi_tcr register bits = ‘10’ or ‘11’) could transmit invalid data or even one word too much.

The error does not occur if the QSPI/SQI module is disabled after the half-duplex receive transfer.

Operations and modes that are affected by this problem

- Mode 0 or 2 of standard Motorola SPI (1-bit)

Operations and modes that are not affected by this problem

- Dual and Quad SPI mode
- SQIROM/XiP mode
- Mode 1 or 3 of standard Motorola SPI (1-bit)

Workaround

This problem can be avoided by one of the following methods

3. Do not use the half-duplex receive mode in standard Motorola SPI (1-bit) mode. Use the full-duplex mode and send dummy data instead.
4. Use SPI mode 1 or 3, if supported by the connected device.
5. Disable and re-enable the QSPI/SQI module after a half-duplex receive transfer (by using the ‘sqi_cr1’ register bit ‘sqi_en’). You have to make sure that the last transfer is finished before disabling the module.

2.5 HIF: Max. MISO hold time is 25 ns at SPI/SQI clock frequencies below 20 MHz (serial DPM)

Issue (Bug)

At SPI clock frequencies below 20 MHz (in all SPI/SQI modes):

When driving MISO, sometimes only a hold time of 25 ns can be guaranteed regarding sample edge. After the hold time, the serial DPM interface invalidates the MISO level up to the next SPI clock setup edge.

This behavior does not occur at SPI clock frequencies greater than or equal to 20 MHz because the half clock period is shorter than the MISO hold time.

Note: The MISO hold value specified in the documentation is wrong!

The exact hold time depends on the number of wait states of read access operations to the netX memory in netX (INTRAM_HS: 0 WS) as well as on the phase shift between SPI clock and internal netX clock.

Operations and modes that are affected by this problem

- Serial DPM at SPI/SQI clock frequencies below 20 MHz

Workaround

Not available

Note: The SPI host should sample the MISO data at sample edge without any problems.
In principal there is a positive hold time and 25 ns should be sufficient.
Serial flash devices typically only require a data hold time of a few nanoseconds.

However, host sampling may take place later than 25 ns after sample edge:
if there are large signal latencies between host and device,
if the host runs at a very low frequency,
if MISO sampling and clock generation are not carried out simultaneously.

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